CLAIMS

1.   A method in a processor comprising steps of:

identifying an instruction loop having a plurality of instructions;

fetching said plurality of instructions from a program memory;

5   storing said plurality of instructions in a register queue;

determining whether said processor requires execution of said instruction loop;

outputting said plurality of instructions from said register queue when said

processor requires execution of said instruction loop;

executing said plurality of instructions.

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2.   The method of claim 1 wherein each of said plurality of instructions in said

instruction loop is a VLIW packet.

3.   The method of claim 1 wherein storing one of said plurality of instructions

15   in said register queue comprises steps of:

adjusting a head pointer to point to a selected register in said register queue;

writing said one of said plurality of instructions into said selected register.

4.   The method of claim 1 wherein said register queue contains a most recently

20   executed plurality of instructions.

5.   The method of claim 1 wherein said step of determining whether said

processor requires execution of said instruction loop comprises checking a PC value.

6.   The method of claim 1 wherein outputting one of said plurality of

instructions from said register queue comprises steps of:

5   adjusting an access pointer to point to a selected register in said register queue;

outputting said one of said plurality of instructions from said selected register.

7.   The method of claim 6 wherein said access pointer is held constant.

10   8.   The method of claim 6 wherein said access pointer is incremented by one.

9.   The method of claim 6 wherein said access pointer is decremented by a

branch interval.

15   10.   The method of claim 1 wherein said program memory comprises a cache.

11.   The method of claim 1 wherein said program memory comprises an

external memory.

20   12.   A circuit in a processor comprising:

an instruction fetch module configured to fetch a plurality of instructions, said

plurality of instructions belonging to an instruction loop in a program memory;

-35-

a register queue configured to store said plurality of instructions;

a tracking module configured to keep track of a desired instruction in said

instruction loop;

an output module configured to output said desired instruction for decoding and

5   execution by said processor.

13.   The circuit of claim 12 wherein each of said plurality of instructions

belonging to said instruction loop is a VLIW packet.

10   14.   The circuit of claim 12 wherein said tracking module comprises a head

pointer configured to point to a selected register in said register queue, wherein said

selected register stores said desired instruction.

15.   The circuit of claim 12 wherein said register queue is configured to contain

15   a most recently executed plurality of instructions.

16.   The circuit of claim 12 wherein said instruction fetch module checks a PC

value to determine whether said processor requires fetching and execution of said

instruction loop.

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17.   The circuit of claim 12 wherein said output module comprises an access

pointer, said access pointer being configured to point to a selected register in said register

queue, wherein said selected register outputs said desired instruction.

18.   The circuit of claim 17 wherein said access pointer is held constant.

5   19.   The circuit of claim 17 wherein said access pointer is incremented by one.

20.   The circuit of claim 17 wherein said access pointer is decremented by a

branch interval.

10   21.   The circuit of claim 12 wherein said program memory comprises a cache.

22.   The circuit of claim 12 wherein said program memory comprises an

external memory.

15   23.   A method in a processor comprising steps of:

identifying a loop having a plurality of VLIW packets;

fetching said plurality of VLIW packets from a program memory;

storing said plurality of VLIW packets in a register queue;

determining whether said processor requires execution of said loop;

20   outputting said plurality of VLIW packets from said register queue when said

processor requires execution of said loop;

executing said plurality of VLIW packets.

24. The method of claim 23 wherein storing one of said plurality of VLIW

packets in said register queue comprises steps of:

adjusting a head pointer to point to a selected register in said register queue;

5   writing said one of said plurality of VLIW packets into said selected register.

25. The method of claim 23 wherein said register queue contains a most

recently executed plurality of VLIW packets.

10   26. The method of claim 23 wherein said step of determining whether said

processor requires execution of said loop comprises checking a PC value.

27. The method of claim 23 wherein outputting one of said plurality of VLIW

packets from said register queue comprises steps of:

15   adjusting an access pointer to point to a selected register in said register queue;

outputting said one of said plurality of VLIW packets from said selected register.

28. The method of claim 27 wherein said access pointer is held constant.

20   29. The method of claim 27 wherein said access pointer is incremented by one.

30. The method of claim 27 wherein said access pointer is decremented by a

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branch interval.

31. The method of claim 23 wherein said program memory comprises a cache.

5   32. The method of claim 23 wherein said program memory comprises an

external memory.

99RSS467